IN THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in this application.

1. (original) A primary processor for a computer system, said primary processor comprising:

a) a main bus;

b) a first processor unit connected to said main bus, said first processor unit having

i) a central processor unit;

ii) a first vector processor unit for performing first matrix calculations, said first vector processor unit connected to said central processor unit to enable said first vector processor unit to operate as a coprocessor for said central processor unit;

c) a second vector processor unit for performing second matrix calculations, said second vector processor unit connected to said main bus;

d) a graphics processor interface for arbitrating whether to transmit from said primary processor calculation results from said first processor unit or from said second vector processor unit, said graphics processor interface connected to said main bus and directly to said second vector processor unit.

2. (original) The primary processor of claim 1, wherein said first matrix calculations comprise calculations for complex modeling of objects for graphical display.

3. (original) The primary processor of claim 2, wherein said second matrix calculations comprise calculations for simple geometrical transformations of objects for graphical display.

4. (original) The primary processor of claim 1, wherein said primary processor is implemented as an integrated circuit on a single substrate.

5. (original) The primary processor of claim 1, wherein said first vector processor unit has at least four floating point processor pipelines.

6. (original) The primary processor of claim 5, wherein said second vector processor unit has at least four floating point processor pipelines.

7. (original) The primary processor of claim 1, wherein said main bus is at least 128-bits wide.

8. (original) The primary processor of claim 7, wherein said central processor unit has an internal bus which is at least 128-bits wide.

9. (original) The primary processor of claim 1, further comprising an image processing unit for decompressing high-resolution texture data from a compressed state.

10. (original) The primary processor of claim 9, wherein said high-resolution texture data is encoded in the MPEG2 format.

11. (original) The primary processor of claim 1, wherein said first vector processor unit includes a first vector interface for decompressing packed data.

12. (currently amended) The primary processor of claim 11, wherein said second vector processor unit includes a second vector interface for decompressing packed data.

13. (original) The primary processor of claim 1, wherein said central processor unit includes a scratchpad memory, said scratchpad memory comprising SRAM and acting as a double buffer between said central processor unit and said main bus.

14. (original) A primary processor for a computer system, said primary processor comprising:

a) a main bus;

b) a coprocessor bus;

c) an interface bus;

d) a central processor unit connected to said main bus and to said coprocessor bus;

e) a first vector processor unit for performing first matrix calculations, said first vector processor being connected to said main bus and directly to said central processing unit through said coprocessor bus to enable said first vector processor unit to operate as a coprocessor for said central processor unit;

f) a second vector processor unit for performing second matrix calculations, said second vector processor unit connected to said main bus and said interface bus;

g) a graphics processor interface for arbitrating whether to transmit from said primary processor calculation results from said first vector processor unit and said central processor unit, or from said second vector processor unit, said graphics processor interface connected to said main bus and directly to said second vector processor unit through said interface bus.

15. (previously presented) The primary processor of claim 14, wherein said first matrix calculations comprise calculations for complex modeling of objects for graphical display.

16. (previously presented) The primary processor of claim 15, wherein said second matrix calculations comprise calculations for simple geometrical transformations of objects for graphical display.

17. (original) The primary processor of claim 14, wherein said primary processor is implemented as an integrated circuit on a single substrate.

18. (original) The primary processor of claim 14, wherein said first vector processor unit has at least four floating point processor pipelines.

19. (original) The primary processor of claim 18, wherein said second vector processor unit has at least four floating point processor pipelines.

20. (original) The primary processor of claim 14, wherein said main bus is at least 128-bits wide.

21. (original) The primary processor of claim 20, wherein said central processor unit has an internal bus which is at least 128-bits wide.

22. (original) The primary processor of claim 14, further comprising an image processing unit for decompressing high-resolution texture data from a compressed state.

23. (original) The primary processor of claim 22, wherein said high-resolution texture data is encoded in the MPEG2 format.

24. (original) The primary processor of claim 14, wherein said first vector processor unit includes a first vector interface for decompressing packed data.

25. (currently amended) The primary processor of claim 24, wherein said second vector processor unit includes a second vector interface for decompressing packed data.

26. (original) The primary processor of claim 14, wherein said central processor unit includes a scratchpad memory, said scratchpad memory comprising SRAM and acting as a double buffer between said central processing unit and said main bus.

27. (previously presented) A computer system comprising:

a) a primary processor as in claim 1;

b) a graphics processor, implemented as an integrated circuit on a single substrate, for rendering three dimensional objects, said graphics processor, comprising

i) a graphics rendering engine;

ii) a local memory;

iii) a mode register for storing first data indicating when said graphics rendering engine is in a first mode corresponding to the receipt by said graphics rendering engine of data calculated by said first vector processor unit and said central processor unit, and for storing second data indicating when said graphics rendering engine is in a second mode corresponding to the receipt by said graphics rendering engine of data calculated by said second vector processor unit;

iv) a plurality of pairs of environmental registers, each of said pairs of environmental registers comprising a first register and a second register, each of said first registers storing data for determining how said graphics rendering engine processes data when said mode register stores said first data indicating said first mode, and each of said second registers storing data for determining how said graphics rendering engine processes data when said mode register stores said second data indicating said second mode; and

c) a graphics transfer bus connecting said graphics processor and said primary processor.

28. (original) A computer system comprising:

a) a primary processor as in claim 14;

b) a graphics processor for rendering three dimensional objects; and

c) a graphics transfer bus connecting said graphics processor and said primary processor.

29. (previously presented) The computer system of claim 28, wherein said graphics processor is implemented as an integrated circuit on a single substrate, and includes:

a) a graphics rendering engine, comprising:

i) a mode register for storing first data indicating when said graphics rendering engine is in a first mode corresponding to the receipt by said graphics rendering engine of data calculated by said first vector processor unit

and said central processor unit, and for storing second data indicating when said graphics rendering engine is in a second mode corresponding to the receipt by said graphics rendering engine of data calculated by said second vector processor unit;

ii) a plurality of pairs of environmental registers, each of said pairs of environmental registers comprising a first register and a second register, each of said first registers storing data for determining how said graphics rendering engine processes data when said mode register indicates said first mode, and each of said second registers storing data for determining how said graphics rendering engine processes data when said mode register indicates said second mode; and

b) a local memory.

30. (previously presented) A graphics processor implemented as an integrated circuit on a single substrate, said graphics processor comprising:

a) a graphics rendering engine, said graphics rendering engine comprising:

i) a mode register for storing first data indicating when said graphics rendering engine is in a first mode corresponding to the receipt by said graphics rendering engine of data calculated by a first vector processor unit and a central processor unit, and for storing second data indicating when said graphics rendering engine is in a second mode corresponding to the receipt by said graphics rendering engine of data calculated by a second vector processor unit;

ii) a plurality of pairs of environmental registers, each of said pairs of environmental registers comprising a first register and a second register, each of said first registers storing data for determining how said graphics rendering engine processes data when said mode register stores said first data indicating said first mode, and each of said

second registers storing data for determining how said graphics rendering engine processes data when said mode register stores said second data indicating said second mode; and

b) a local memory.

31. (original) The graphics processor of claim 30, wherein said graphics rendering engine includes logic circuitry for implementing alpha blending.

32. (previously presented) The graphics processor of claim 30, wherein said graphics rendering engine includes logic circuitry for implementing fogging.

33. (original) The graphics processor of claim 30, wherein said graphics rendering engine includes logic circuitry for a depth test to implement Z-buffering.

34. (original) The graphics processor of claim 30, wherein said graphics rendering engine includes logic circuitry for implementing a destination alpha test.

35. (original) The graphics processor of claim 30, wherein said graphics rendering engine includes logic circuitry for implementing an alpha test.

36. (original) The graphics processor of claim 30, wherein said local memory includes a frame buffer, a texture buffer, and a z-buffer.

37. (previously presented) The graphics processor of claim 36, wherein said graphics rendering engine includes logic circuitry for filling said frame buffer with a rectangle of at least 16 pixels per clock cycle, and wherein said rectangle can be initiated at a different column for each row of a single polygon being rendered.

38. (previously presented) The graphics processor of claim 36, wherein said graphics rendering engine includes logic circuitry for implementing a moving stamp in writing to said frame buffer.

39. (previously presented) A method of performing graphics calculations comprising the steps of:

a) performing first calculations in a first data stream using a first processor, wherein said first calculations comprise calculations for complex modeling of objects for graphical display;

b) simultaneously performing second calculations in a second data stream using a second processor, wherein said second data stream is parallel to said first data stream and said second calculations comprise calculations for simple geometrical transformations of objects for graphical display.

40. (original) The method of claim 39, further comprising the step of arbitrating whether said first calculations or said second calculations are transmitted to a graphics processor at any given time.

41. (canceled)

42. (previously presented) A method of programming a graphics program comprising the steps of:

a) designating first calculations to be processed by a first processor, wherein said first calculations comprise calculations for complex modeling of objects for graphical display;

b) designating second calculations to be calculated by a second processor, wherein said second calculations comprise calculations for simple geometrical transformations of objects for graphical display; and

c) processing said first calculations and said second calculations simultaneously; and

d) arbitrating whether said first calculations or said second calculations are transmitted to a graphics processor at any given time.

43. (canceled)

44. (previously presented) A system for performing graphics calculations comprising:

a) a first processor for performing first calculations and transmitting said first calculations in a first data stream, said first calculations comprising calculations for complex modeling of objects for graphical display;

b) a second processor for performing second calculations and transmitting said second calculations in a second data stream, said second data stream being parallel to said first data stream and said second calculations comprising calculations for simple geometrical transformation of objects for graphical display.

45. (previously presented) A system as in claim 44, further comprising an interface circuit for receiving said first data stream and said second data stream and for determining whether said first data stream or said second data stream is transmitted to a third processor for rendering.

46. (currently amended) A system for performing graphics calculations comprising:

a) a first processor for performing first graphics calculations and transmitting said first graphics calculations in a first data stream;

b) a second processor for performing second graphics calculations and transmitting said second graphics calculations in a second data stream;

c) an interface circuit for receiving said first data stream and said second data stream and for determining whether said first data stream or said second data stream is transmitted to a third processor for rendering~~.~~;

wherein said first graphics calculations comprise calculations for complex modeling of objects for graphical display and said second graphics calculations comprise

calculations for simple geometrical transformations of objects for graphical display.

47. (canceled)